Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

APPLICATION NOTE

ABSTRACT
As general purpose components, logic devices are used at different frequencies and power supply voltages in many different varieties of applications. This large diversity has produced the need to express a single parameter that can be used in determining the power dissipation of a device in a given applications. This application note describes different components of power dissipation and how they may be calculated.

AN263

Power considerations when using CMOS and BiCMOS logic devices

Michael Lyons

2002 Mar 01

Philips Semiconductors

PHILIPS

Power considerations when using CMOS and BiCMOS logic devices

AN263

Author: Michael Lyons

INTRODUCTION

As general purpose components, logic devices are used at different frequencies and power supply voltages in many different varieties of applications. This large diversity has produced the need to express a single parameter that can be used in determining the power dissipation of a device in a given application.

This application note describes different components of power dissipation and how they may be calculated.

1. STATIC CONSIDERATIONS

1.1 CMOS

When a CMOS device is not switching and the input levels are GND or V_{CC}, the p-channel and n-channel transistors do not conduct at the same time; no direct MOS transistor channel path exists between V_{CC} & GND. In practice however, thermally generated minority carriers, which are present in all reverse biased diode junctions, allow a very small leakage current to flow between V_{CC} and GND. As this leakage current is typically a few nA, quiescent CMOS power dissipation is extremely low. Maximum quiescent power dissipation for the above conditions is calculated as:

$$P_D = V_{CC} \times I_{CC} \quad (1)$$

Where:

I_{CC} is specified in the device datasheet.

1.2 BiCMOS

In the case of BiCMOS devices; the current in the output bipolar stage is different when the output is set high or low. This results in two datasheet specifications for quiescent current I_{CCL} & I_{CCH}. Quiescent power dissipation for input levels of GND or V_{CC} is calculated as:

$$P_D = V_{CC} \times (n_1 I_{CCL} + n_2 I_{CCH})/(n_1 + n_2) \quad (2)$$

Where:

n1 is the number of outputs LOW
n2 is the number of outputs HIGH

1.3 Input stage current due to GND < V_I < V_{CC}

In the case where the input levels of the device are not held at GND or V_{CC}, a direct MOS transistor current path can exist between V_{CC} and GND; this leads to additional supply current through the input buffer stage of both CMOS and BiCMOS devices, and additional power dissipation. In device datasheets this is represented as ΔI_{CC}, the additional current due to an input level other than V_{CC} or GND. In the case of 5.5 V logic families this parameter is generally measured at an input voltage of V_{CC} – 2.1; in the case of 3.3 V logic families it's measured at an input voltage of V_{CC} – 0.6 V. Static power dissipation is then calculated as:

$$P_D = V_{CC} \times [(n_1 I_{CCL} + n_2 I_{CCH})/(n_1 + n_2) + n\Delta I_{CC}] \quad (3)$$

Where:

n is the number of inputs at the intermediate level.

Note: For CMOS $I_{CCL} = I_{CCH} = I_{CC}$, simplifying Equation (3).

Table 1 shows a comparison of I_{CC} and ΔI_{CC} for the '244 function of several logic families.

Table 1. Specified I_{CC} and ΔI_{CC} for CMOS and BiCMOS families

CMOS families						
Device	**Voltage**	**$I_{CC}Q$**		**V_I**	**ΔI_{CC}**	**Units**
74HC244	6 V	80		V_{CC}–2.1 V	450	µA
74AHC244	5.5 V	40		V_{CC}–2.1 V	1500	µA
74LV244	5.5 V	20		V_{CC}–0.6 V	500	µA
74LVC244	3.6 V	10		V_{CC}–0.6 V	500	µA
74ALVC244	3.6 V	10		V_{CC}–0.6 V	750	µA
BiCMOS families						
Device	**Voltage**	**I_{CCZ}**	**I_{CCL}**	**I_{CCH}**	**V_I**	**ΔI_{CC}**	**Units**
74ABT244	5.5 V	0.25	30	0.25	V_{CC}–2.1 V	1.5	mA
74LVT244	3.6 V	0.19	12	0.19	V_{CC}–0.6 V	0.2	mA

2. DYNAMIC CONSIDERATIONS

When a device is clocked, power is dissipated through the charging and discharging of on-chip parasitic and load capacitances. Power is also dissipated at the moment the output switches when both the p-channel and the n-channel transistors are partially conducting. This transient energy loss is typically only 10% of that due to parasitic capacitance.

The total dynamic power dissipation per device is:

$$P_D = \Sigma(C_{PD}V_{CC}^2 f_I) + \Sigma(C_L V_{CC}^2 f_O) \quad (4)$$

Where:

C_{PD} is the power dissipation capacitance per buffer
f_I is the input frequency
f_O is the output frequency
C_L is the total external load capacitance per output.

It should be noted from the Equation (4), that C_{PD} is a useful parameter for determining power dissipation in any device for which power dissipation is a linear function of frequency. Figure 1 shows I_{CC} as a function of frequency for the devices listed in Table 1. From this we can conclude that for all of Philips' CMOS and BiCMOS logic families C_{PD} can be used in order to determine the worst case power consumption of a device in a given application.

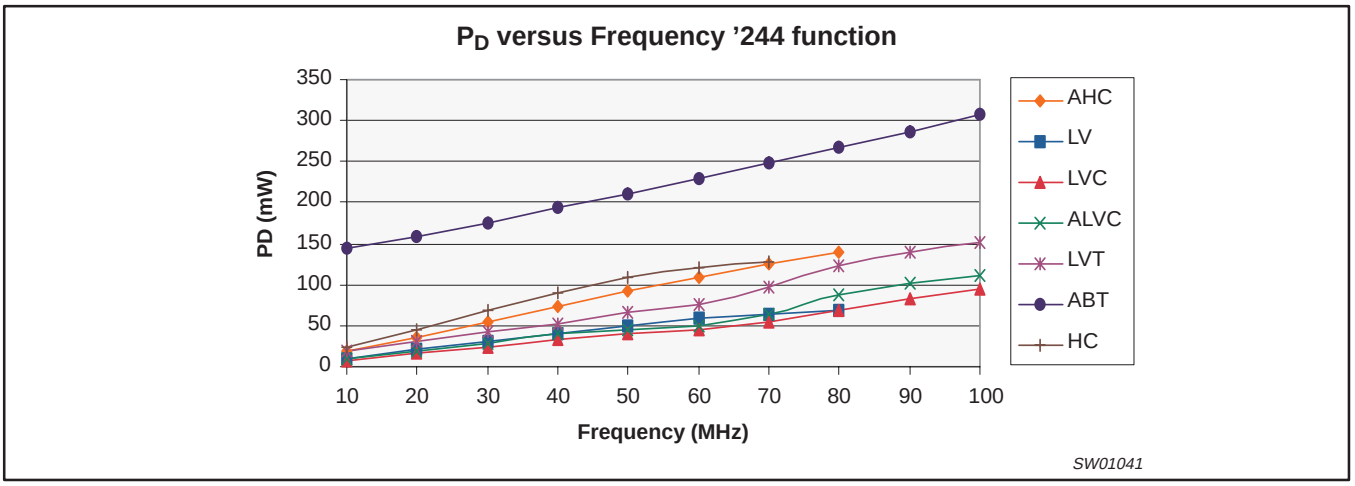

Figure 1. Power dissipation as a function of frequency.

2.1 Duty cycle considerations with unbalanced outputs

In the case of unbalanced output drive, such as is found in BiCMOS, the output duty cycle could also be considered. Figure 2 shows the effect of duty cycle on the power dissipation of the 74LVT244. It can be concluded from these measurements that the duty cycle has little effect on the total power dissipation. This is due to the switching currents within BiCMOS products being more dominant than steady state currents.

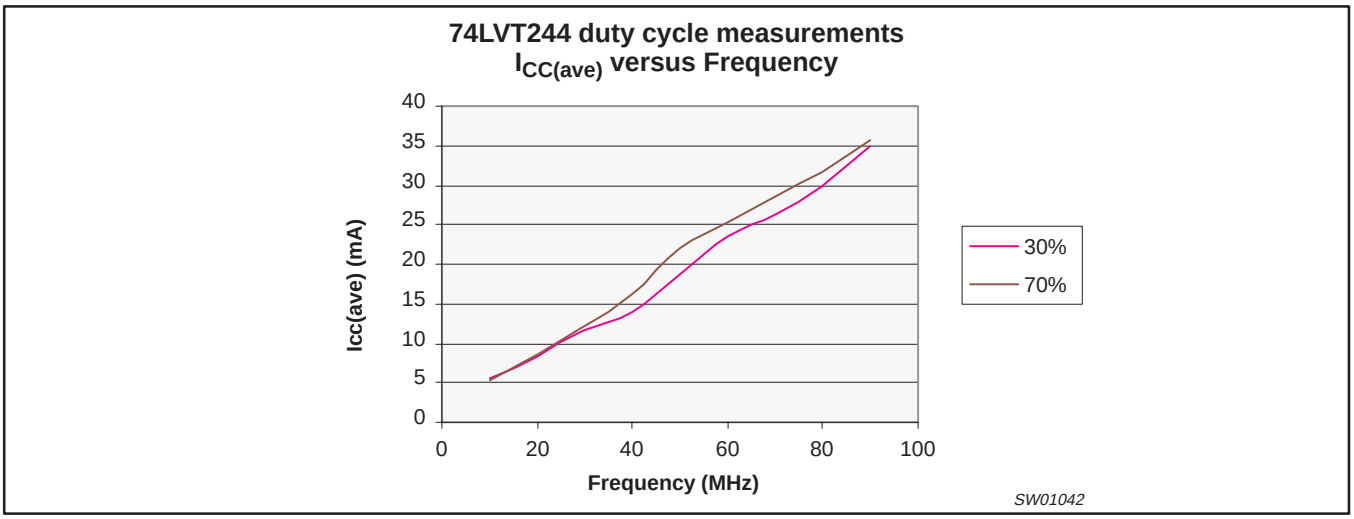

Figure 2. Effect of duty cycle on Average current versus Frequency.

2.2 Power dissipation due to slow input rise/fall times

When an output stage switches, there is a brief period when both output transistors conduct. The resulting through-current is additional to the normal supply current and causes power dissipation to increase linearly with the input rise or fall time. As long as the input voltage is less than the n-channel transistor threshold voltage, or is higher than V_{CC} minus the p-channel transistor threshold voltage, one of the input transistors is always off and there is no through-current. When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current flows, reaching a maximum at $V_I = 0.5\ V_{CC.}$ For devices with CMOS inputs, the maximum current is determined by the geometry of the input transistors. When Schmitt triggers are used to square pulses with long rise/fall times, through-current at the Schmitt-trigger inputs will increase the power dissipation (see Schmitt-trigger data sheets).

3. POWER DISSIPATION CAPACITANCE

C_{PD} is specified in the CMOS device data sheets, the published values being calculated from the results of tests described in this section. The test set-up is shown in Figure 3. The worst-case operating conditions for C_{PD} are always chosen and the maximum number of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet. **Appendix 1** gives the pin status for devices during a C_{PD} test. Devices that can be separated into independent sections are measured per section, the others are measured per device.

The recommended test frequency for determining C_{PD} is 10 MHz, 50% duty cycle. Loading the switched outputs gives a more realistic value of C_{PD}, because it prevents transient through-current in the output stages.

The values of C_{PD} provided in datasheets have been calculated using:

$$C_{PD} = \frac{(I_{CC(ave)} \times V_{CC}) - [(C_L \times V_{CC}{}^2 \times f_O) + V_{CC} \times I_{STAT}]}{V_{CC}{}^2 \times f_I} \quad (5)$$

Where:

C_{PD} = power dissipation capacitance (per buffer)
$I_{CC(ave)}$ = supply current
V_{CC} = supply voltage
C_L = output load capacitance
f_O = output frequency
f_I = input frequency
I_{STAT} = supply current at dc (approx. zero for CMOS)

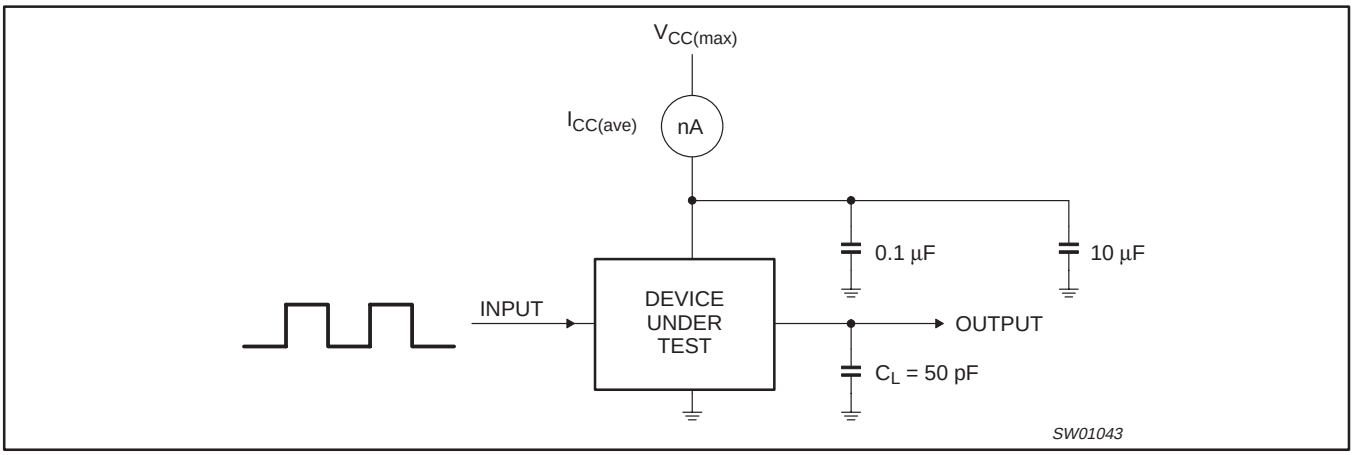

Figure 3. Test set-up for C_{PD} determination.

3.1 Example C_{PD} calculations

CMOS:
In the case of 74LVC244, I_{STAT} is negligible and can be considered as zero for the purpose of C_{PD} calculation. The test set-up for the '244 as indicated in **Appendix 1** was used, with the load shown in Figure 3. At V_{CC} = 3.6 V, f_I = 10 MHz; $I_{CC(ave)}$ was found to be 2.24 mA.

Using Equation (5):

$$C_{PD} = \frac{(2.24\ mA \times 3.6\ V) - [(50\ pF \times 3.6\ V^2 \times 10\ MHz) + 0\ mW]}{3.6\ V^2 \times 10\ MHz}$$

$$C_{PD} = 12.2\ pF$$

BiCMOS:
In the case of 74LVT244, I_{STAT} cannot be considered as negligible at low frequency. As a result, a higher frequency is recommended for modeling its C_{PD}. The test set-up for the '244 as indicated in **Appendix 1** was used to perform a measurement, with the same load shown in Figure 3, however at a frequency of 30 MHz. $I_{CC(ave)}$ was found to be 11.53 mA. We then apply Equation (5) with the assumption that I_{STAT} is negligible.

Using Equation (5):

$$C_{PD} = \frac{(11.53\ mA \times 3.6\ V) - (50\ pF \times 3.6\ V^2 \times 30\ MHz)}{3.6\ V^2 \times 30\ MHz}$$

$$C_{PD} = 56.8\ pF$$

Note: Performing the measurement and calculation at 20 MHz results in a C_{PD} of 66 pF. Due to the uncertainty of I_{STAT} in a given configuration, it is recommended that a 5 to 10% guardband is used when approximating power dissipation for BiCMOS devices.

4. USING C_{PD} TO CALCULATE POWER DISSIPATION

4.1 CMOS Device Calculation

Consider a 3.6 V application in which every 40 ms a 74LVC244A device is used to buffer four 40 MHz, 75% positive duty cycle signals and two 80 MHz, 75% positive duty cycle signals, for a duration of 25 ms. The unused inputs are tied to 3.6 V, the outputs drive 30 pF loads, and when not buffering, four inputs are held at 3.0 V and two inputs held at GND.

In calculating the average power dissipation we need to consider both the power dissipation for the 15 ms when the device is not buffering, and the power dissipation for the 25 ms when the buffers are active.

In the first 15 ms the device is static and power dissipation is calculated using Equation (2). In this case we have four inputs that are connected to V_{CC} – 0.6 V.

$$\begin{aligned} P_{D1} &= 3.6 \times 10\ \mu A + 4 \times 3.6 \times 500\ \mu A \\ &= 7.24\ mW \end{aligned}$$

In the second 25 ms the total power dissipation can be estimated as the combination of static the dynamic dissipation due to the four buffers and outputs switching at 40 MHz, and dynamic dissipation due to the two buffers and outputs switching at 80 MHz.

$$\begin{aligned} P_{D2} &= 4 \times (C_{PD} + C_L) \times 3.6^2 \times 40\ MHz + 2 \times (C_{PD} + C_L) \times 3.6^2 \times 80\ MHz \\ &= 87.1\ mW + 87.1\ mW \\ &= 174.2\ mW \end{aligned}$$

The average power dissipation is then:

$$\begin{aligned} P_{D(ave)} &= (15 \times 7.24\ mW + 25 \times 174.2\ mW) / 40 \\ &= 111.6\ mW \end{aligned}$$

4.2 BiCMOS Device Calculation

Consider the LVT244 in the same application.

In the case of BiCMOS devices, the duty cycle must be taken into consideration because I_{CCL} and I_{CCH} are not identical. In the first 15 ms of the application the static power dissipation is calculated using Equation (2) to determine quiescent power dissipation and adding the power dissipation caused by the four inputs that are connected to V_{CC} – 0.6 V.

$$P_{D1} = 3.6 \times (6 \times I_{CCH} + 2 \times I_{CCL}) / 8 + 4 \times 3.6 \times \Delta I_{CC}$$
$$= 11.3 \text{ mW} + 2.9 \text{ mW}$$
$$= 14.2 \text{ mW}$$

The power dissipation in the next 25 ms contains in addition to those of the 74LVC244A case the component I_{STAT}. P_{D1} can be used to approximate I_{STAT}.

$$P_{D2} = 4 \times (C_{PD} + C_L) \times 3.6^2 \times 40 \text{ MHz} + 2 \times (C_{PD} + C_L) \times 3.6^2 \times 80 \text{ MHz} + 3.6 \times I_{STAT}$$
$$= 180 \text{ mW} + 180 \text{ mW} + 14.2 \text{ mW}$$
$$= 374.2 \text{ mW}$$

It should be noted that in using equation 3 to determine our dynamic dissipation components we are assuming a rail to rail output swing. As BiCMOS outputs don't swing rail to rail this will produce a worse case approximation.

The calculated average power dissipation is then:

$$P_{D(ave)} = (15 \times 14.2\text{mW} + 25 \times 374.2 \text{ mW}) / 40$$
$$= 239.2 \text{ mW}$$

RESULTS AND CONCLUSION

Table 2. Comparison of measured and calculated results

Device	Static 15 ms			Dynamic 25 ms			Total	
	$I_{CC(ave)}$ (mA)	P_{D1} (mW)		$I_{CC(ave)}$ (mA)	P_{D2} (mW)		$P_{D(ave)}$ (mW)	
		Measured	Calculated		Measured	Calculated	Measured	Calculated
74LCV244A	0.008	0.028	7.24	48.2	173.5	174.2	108.4	111.6
74LVT244	2.5	9	14.2	102.4	368.6	374.2	233.8	239.2

Determination of power dissipation is an essential part of system design. By understanding the static and dynamic components of power dissipation, and how they can be modeled; a system designer is able to estimate the worse case power dissipation of an application.

Table 2 shows the comparison of the measured results to those calculated. The values of static and dynamic current that were calculated are within 10% of the measured values. Importantly the calculated values are higher than the measured values. This is due to the calculations being made with worse case datasheet limits. This is considered advantageous in system level power calculations, as it provides extra power budget margin in the application. It can be concluded, from the examples presented, that any device that has a linear relationship between supply current and frequency can be modeled as a single power dissipation capacitance C_{PD} for the purpose of power dissipation calculations of that device used in any application.

REFERENCES

[1] *HCMOS users guide*, January 1986.

[2] *AN241: Thermal Considerations for Advanced Logic Families*, June 1992.

APPENDIX 1: CONDITIONS FOR C_{PD} TESTS

Gates. All inputs except one are held at either V_{CC} or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency. C_{PD} is specified per-gate.

Decoders. One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to V_{CC} or GND, whichever enables operation. C_{PD} is specified per-independent-decoder.

Multiplexers. One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the outputs to toggle. With 3-State multiplexers, C_{PD} is specified per output function for enabled outputs.

Bilateral switches. The switch inputs and outputs are open-circuit. With the enable input active, one of the select inputs is toggled, the others are tied HIGH or LOW. C_{PD} is specified per switch.

3-State buffers and transceivers. C_{PD} is specified per buffer with the outputs enabled. Measurement is as for simple gates.

Latches. The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one latch is toggled by the clock. 3-State latches are measured with their outputs enabled. C_{PD} is specified per-latch.

Flip-flops. Measurement is performed as for latches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

Shift registers. The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at V_{CC} or GND. 3-State devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

Counters. A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for C_{PD} are given for each counter in the device.

Arithmetic circuits. Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

Display drivers. C_{PD} is not normally required for LED drivers because LEDs consume so much power as to make the effect of C_{PD} negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. When it is needed, C_{PD} is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs. If either type of driver (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

One-shot circuits. In some cases, when the device I_{CC} is significant, C_{PD} is not specified. When it is specified, C_{PD} is measured by toggling one trigger input to make the output a square wave. The timing resistor is tied to a separate supply (equal to V_{CC}) to eliminate its power contribution.

Pin conditions for C_{PD} tests

Function	Pin Number																											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
02	C	P	L	O	D	D	G	D	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
03	P	H	B	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
04	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
U04	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
08	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
10	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
11	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
14	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
20	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
21	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
27	P	L	D	D	D	O	G	O	D	D	D	C	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
30	P	H	H	H	H	H	G	C	O	O	H	H	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
32	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
42	C	C	O	O	O	O	O	G	O	O	O	L	L	L	P	V	–	–	–	–	–	–	–	–	–	–	–	–
58	P	D	D	D	D	O	G	O	L	L	L	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
73	P	H	H	V	D	D	D	O	O	D	G	C	C	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
74	H	Q	P	H	C	C	G	O	O	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
75	C	Q	D	D	V	D	D	O	O	O	O	G	P	O	O	C	–	–	–	–	–	–	–	–	–	–	–	–
85	L	H	P	H	O	C	O	G	L	L	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
86	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
93	Q	L	L	D	V	D	D	C	C	G	C	C	D	P	–	–	–	–	–	–	–	–	–	–	–	–	–	–
107	H	C	C	H	O	O	G	D	D	D	D	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
109	H	H	L	P	H	C	C	G	O	O	D	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
112	P	H	H	H	C	C	O	G	O	D	D	D	D	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
123	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
125	L	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
126	H	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
132	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
137	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
138	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
139	L	P	L	C	C	O	O	G	O	O	O	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
147	H	H	H	H	H	O	O	G	C	H	P	H	H	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
151	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
153	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
154	C	C	O	O	O	O	O	O	O	O	O	G	O	O	O	O	O	L	L	L	L	L	P	V	–	–	–	–
157	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
158	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
160	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
161	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
162	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
163	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
164	Q	H	C	C	C	C	G	P	H	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
165	H	P	D	D	D	D	C	G	C	Q	D	D	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
166	Q	D	D	D	D	L	P	G	H	D	D	D	C	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
173	L	L	C	O	O	O	P	G	L	L	D	D	D	Q	L	V	–	–	–	–	–	–	–	–	–	–	–	–
174	H	C	Q	D	O	D	O	G	P	O	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–
175	H	C	C	Q	D	O	O	G	P	O	O	D	D	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
181	P	H	H	L	L	H	H	L	C	C	C	G	C	B	C	C	C	L	H	L	H	L	H	V	–	–	–	–
182	H	L	H	L	H	L	O	G	C	O	C	C	P	H	L	V	–	–	–	–	–	–	–	–	–	–	–	–
190	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
191	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
192	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	–	–	–	–	–	–	–	–	–	–	–	–
193	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	–	–	–	–	–	–	–	–	–	–	–	–
194	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
195	H	H	L	D	D	D	D	G	H	P	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
221	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
237	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
238	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
240	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–

Pin conditions for C_{PD} tests (continued)

Function	Pin Number																											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
241	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	H	V	–	–	–	–	–	–	–	–
242	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
243	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
244	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–
245	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
251	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
253B	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
257	P	L	H	C	D	D	O	G	O	D	D	O	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
258	P	L	H	C	D	D	O	G	O	D	D	O	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
259	L	L	L	C	O	O	O	G	O	O	O	O	Q	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–
7266	P	L	C	O	D	D	G	D	D	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
273	H	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
280	L	L	O	L	C	C	G	P	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
283	C	H	L	C	P	H	L	G	C	C	H	L	C	L	H	V	–	–	–	–	–	–	–	–	–	–	–	–
297	H	H	H	P	Q	L	C	G	D	D	O	O	D	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–
299	H	L	L	C	C	C	C	C	H	G	Q	P	C	C	C	C	C	D	L	V	–	–	–	–	–	–	–	–
354	D	D	D	D	D	D	L	H	L	G	L	L	L	P	L	L	H	C	C	V	–	–	–	–	–	–	–	–
356	D	D	D	D	D	D	D	Q	P	G	L	L	L	L	L	L	H	C	C	V	–	–	–	–	–	–	–	–
365	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
366	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
367	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
368	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
373	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
374	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
377	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
390	P	L	C	Q	C	C	C	G	O	O	O	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
393	P	L	C	C	C	C	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
423	L	P	H	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
533	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
534	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
540	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
541	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
563	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
564	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
573	L	P	D	D	D	D	D	D	D	G	H	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
574	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
583	H	H	H	L	L	C	C	G	C	C	C	H	P	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
597	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–	–
7597	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–	–
640	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
643	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
646	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
648	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
670	Q	Q	Q	L	P	C	C	G	C	C	L	L	L	P	Q	V	–	–	–	–	–	–	–	–	–	–	–	–
688	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	C	V	–	–	–	–	–	–	–	–
4002	C	P	L	L	L	O	G	O	D	D	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4015	P	C	O	O	O	D	D	G	D	O	C	C	C	L	Q	V	–	–	–	–	–	–	–	–	–	–	–	–
4016	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4017	C	C	C	C	C	C	C	G	C	C	C	C	L	P	L	V	–	–	–	–	–	–	–	–	–	–	–	–
4020	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4024	P	L	C	C	C	C	G	O	C	O	C	C	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4040	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4046A	O	C	L	O	H	O	O	G	O	O	O	O	O	P	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4049	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–	–	–	–	–	–	–
4050	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–	–	–	–	–	–	–
4051	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4052	O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4053	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4059	P	D	H	L	L	L	L	L	L	L	H	G	H	H	L	L	L	L	L	L	L	L	C	V	–	–	–	–
4060	C	C	C	C	C	C	C	G	C	C	P	L	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–

Pin conditions for C_{PD} tests (continued)

Function	Pin Number																											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
4066	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4067	O	O	O	O	O	O	O	O	O	P	L	G	L	L	L	O	O	O	O	O	O	O	O	V	–	–	–	–
4075	P	L	D	D	D	O	G	L	C	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4094	H	Q	P	C	C	C	C	G	C	C	C	C	C	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
4316	O	O	O	O	P	D	L	G	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4351	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–	–	–	–	–
4352	O	O	O	O	O	O	L	H	G	G	H	P	L	O	O	O	O	O	O	V	–	–	–	–	–	–	–	–
4353	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–	–	–	–	–
4510	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–
4511	L	L	H	H	L	L	P	G	C	C	O	O	C	O	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4514	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–	–	–
4515	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–	–	–
4516	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–
4518	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4520	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4538	G	R	H	P	H	C	C	G	O	O	D	D	L	O	G	V	–	–	–	–	–	–	–	–	–	–	–	–
4543	H	L	L	H	L	P	L	G	C	C	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
7030	G	G	C	P	Q	Q	Q	Q	Q	Q	Q	Q	Q	G	L	C	C	C	C	C	C	C	C	C	C	P	H	V
7046A	O	C	L	O	H	O	O	G	O	O	O	O	O	P	O	V	–	–	–	–	–	–	–	–	–	–	–	–
40102	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
40103	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
40104	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
40105	L	C	P	Q	Q	Q	Q	G	L	C	C	C	C	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–

Pin conditions for C_{PD} tests (continued)

Function	Pin Definition																											
16240	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	D	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	P	D	–	–	–	–	–	–	–	–
16241	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	D	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	P	D	–	–	–	–	–	–	–	–
16244	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	D	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	P	D	–	–	–	–	–	–	–	–
16245	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	P	D	G	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	D	D	D	O	O	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	C	L	–	–	–	–	–	–	–	–
16260	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	H	D	G	D	D	V	C	O	O	G	O	O	O	O	O	O	G	O	O	O	V	P	D	G	D	H	H
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	H	D	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	D	D	H
16273	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	L	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	Q	P	–	–	–	–	–	–	–	–
16373	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	D	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	Q	P	–	–	–	–	–	–	–	–
16374	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	D	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	Q	P	–	–	–	–	–	–	–	–
16500	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	P	Q	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	D	H	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	G	D	O	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	C	D	G
16501	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	P	Q	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	D	H	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	G	D	O	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	C	D	G
16540	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	D	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	P	L	–	–	–	–	–	–	–	–
16541	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	O	D	D	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	P	D	–	–	–	–	–	–	–	–

Pin conditions for C_{PD} tests (continued)

Function	Pin Definition																											
16543	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	P	L	G	Q	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	L	L	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	H	H	H	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	C	G	H	H	H
16600	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	L	Q	G	Q	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	L	L	H
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	H	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	C	G	C	P	L
16601	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	L	Q	G	Q	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	L	L	H
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	H	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	C	G	C	P	L
16623	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	P	D	G	D	D	V	D	D	G	D	D	D	D	G	D	D	V	D	D	G	D	D	L	L	O	O	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	O	O	V	O	O	G	O	O	O	O	G	O	O	V	O	O	G	O	C	L	–	–	–	–	–	–	–	–
16646	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	D	P	G	Q	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	L	D	H
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	L	D	D	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	C	G	D	D	L
16652	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	D	P	G	Q	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	L	D	H
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	H	D	D	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	C	G	D	D	H
16731	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	G	O	O	G	C	C	V	P	D	D	D	L	L	H	D	D	D	D	G	O	O	V	O	O	G	O	O	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	V	O	O	G	O	O	V	O	O	G	O	O	G	O	O	V	O	O	G	O	O	V	O	O	G	O	O	V
16821	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	O	O	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	D	Q	P
16823	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	L	C	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	O	L	H
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	L	D	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	Q	L	P
16825	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	O	O	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	L	D	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	D	P	L
16827	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	O	O	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	L	D	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	D	P	L
16835	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	D	D	C	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	O	L	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	G	P	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	Q	D	G

Pin conditions for C_{PD} tests (continued)

Function	Pin Definition																											
16841	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	C	O	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	O	O	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	H	D	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	D	P	H
16843	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	L	C	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	O	G	O	L	H
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	H	H	D	G	D	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	P	H	H
16899	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	D	L	C	G	O	O	O	O	V	O	O	O	D	D	G	D	D	O	O	O	V	O	O	O	O	G	O	P
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	H	D	G	D	D	D	D	V	D	D	D	D	D	G	D	D	D	D	D	V	D	D	D	D	G	Q	H	L
16952	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	L	P	L	G	Q	D	V	D	D	D	G	D	D	D	D	D	D	G	D	D	D	V	D	D	G	L	D	L
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	H	D	H	G	O	O	V	O	O	O	G	O	O	O	O	O	O	G	O	O	O	V	O	C	G	H	D	H
164245	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	H	C	O	G	O	O	V1	O	O	G	O	O	O	O	G	O	O	V1	O	O	G	O	O	H	L	D	D	G
	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
	D	D	V2	D	D	G	D	D	D	D	G	D	D	V2	D	D	G	D	P	L	–	–	–	–	–	–	–	–

NOTE:
For 32-bit devices, the C_{PD} set-up of control pins is identical to those of the 16-bit equivalent. The extra inputs are set as D, the extra outputs as O.

KEY

V = V_{CC} (in the case of level translators V1 = 5.5 V, V2 = 3.6 V)
G = ground
H = logic 1 (V_{CC})
L = logic 0 (ground)
D = don't care (input either H or L but not switching)
C = 50 pF load to ground
O = an open pin (50 pF to ground is allowed)
P = input pulse (see Figure 4)
Q = half frequency pulse (see Figure 4)
R = 1 kΩ pull-up resistor to an additional supply (not V_{CC})
B = both R and C

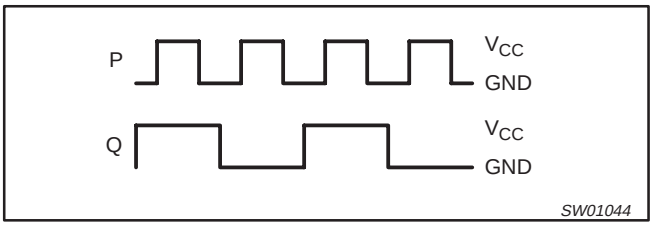

Figure 4.

NOTES

Power considerations when using CMOS and BiCMOS logic devices

AN263

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2002
All rights reserved. Printed in U.S.A.

Date of release: 03-02

Document order number: 9397 750 09511

Let's make things better.

Philips Semiconductors

PHILIPS